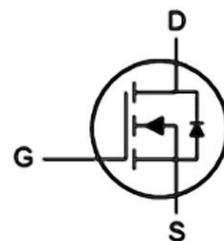
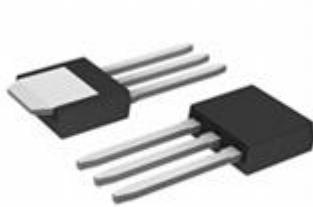


Description

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

Features

- 1) $V_{DS}=60V, I_D=50A, R_{DS(ON)} < 20m\Omega @ V_{GS}=10V$
 - 2) Low gate charge.
 - 3) Green device available.
 - 4) Advanced high cell density trench technology for ultra $R_{DS(ON)}$.
 - 5) Excellent package for good heat dissipation.
-



Absolute Maximum Ratings $T_c=25^\circ C$, unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current-	50	A
	Continuous Drain Current- $T_c=100^\circ C$	35.4	
	Pulsed Drain Current ¹	-	
E_{AS}	Single Pulse Avalanche Energy ²	300	mJ
P_D	Power Dissipation $T_c=25^\circ C / T_c=100^\circ C$	85	W
		-	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	°C/W



RYN60FAC

Package Marking and Ordering Information

Part NO.	Marking	Package
RYN60FAC	RYN60FAC	TO-251

Electrical Characteristics $T_c=25^\circ\text{C}$ unless otherwise noted

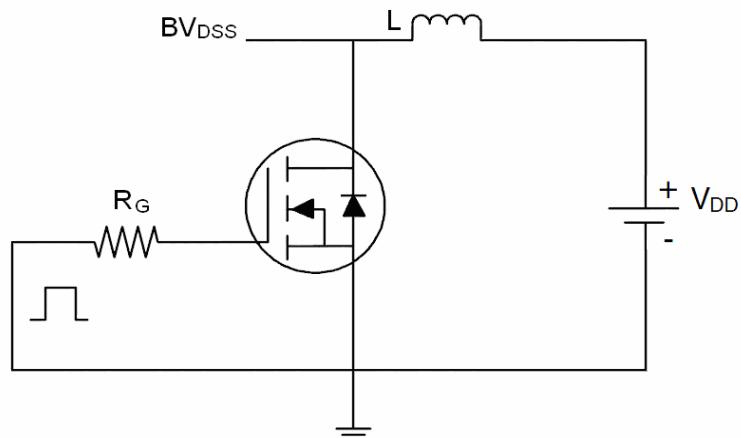
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250 \mu\text{A}$	60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=60\text{V}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
On Characteristics						
$V_{\text{GS}(\text{th})}$	GATE-Source Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}, I_{\text{D}}=250 \mu\text{A}$	1.4	1.9	2.5	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On Resistance ³	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	---	14	20	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$	---	---	---	
G_{FS}	Forward Transconductance	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=20\text{A}$	18	-	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{D}}=30\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	---	2050	--	pF
C_{oss}	Output Capacitance		---	158	---	
C_{rss}	Reverse Transfer Capacitance		---	120	---	
R_g	Gate Resistance	f=1MHz	---	--	-	Ω
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn-On Delay Time ³	$V_{\text{DD}}=30\text{V}, I_{\text{D}}=-A,$ $V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=3 \Omega$	---	7.4	---	ns
t_r	Rise Time ^{2,3}		---	5.1	---	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	28.2	---	ns
t_f	Fall Time ^{2,3}		---	5.5	---	ns
Q_g	Total Gate Charge ³	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=30\text{V},$ $I_{\text{D}}=20\text{A}$	---	50	30	nC
Q_{gs}	Gate-Source Charge		---	6	---	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	15	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ³	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}, T_j=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time ³	$I_{\text{F}}=20\text{A}, di/dt=100\text{A}/\mu\text{s}$	---	48	--	ns
Q_{rr}	Reverse Recovery Charge		---	40	---	nC

Notes:

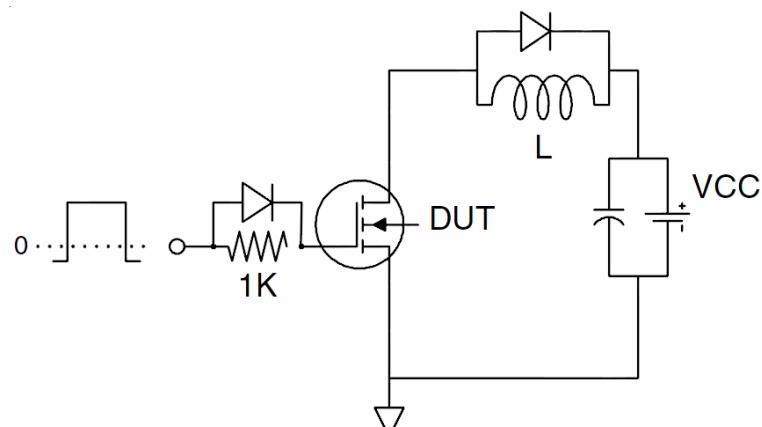
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_j=25^\circ\text{C}, V_{\text{DD}}=30\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

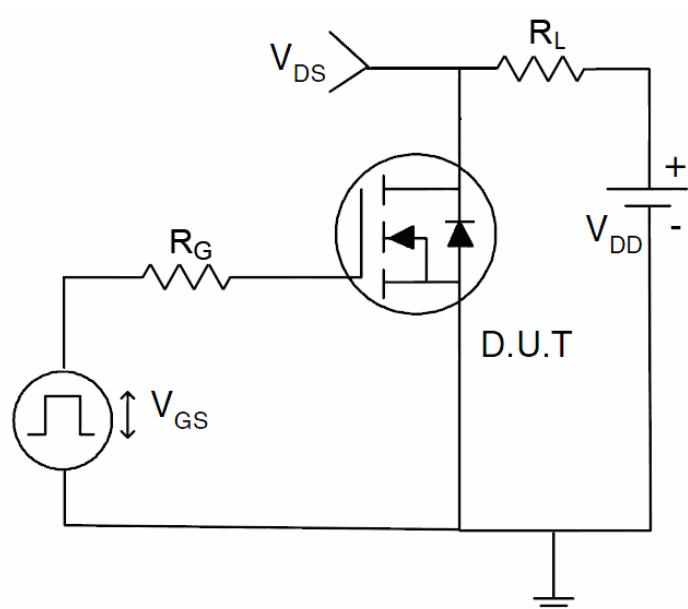
1) E_{AS} test Circuit

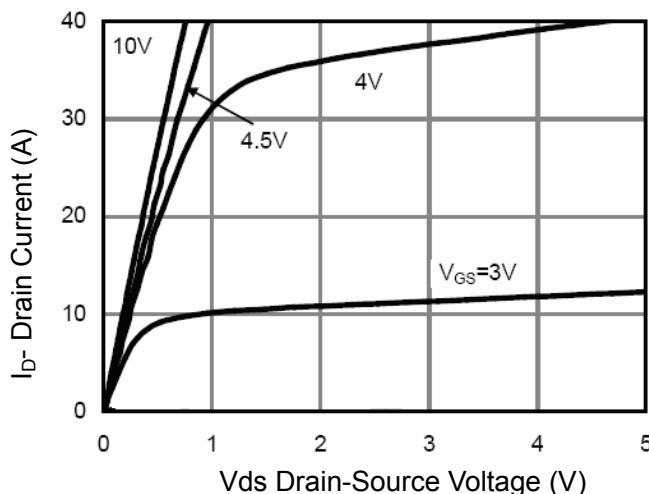
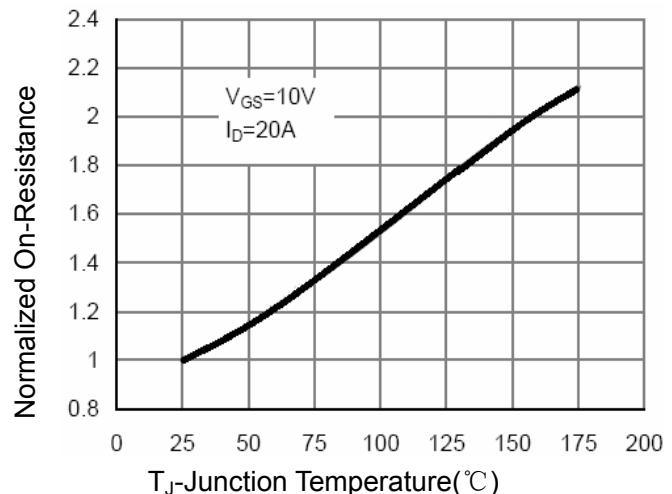
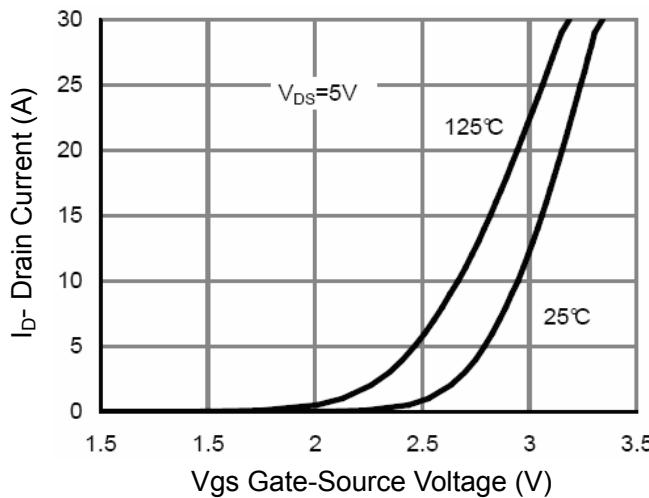
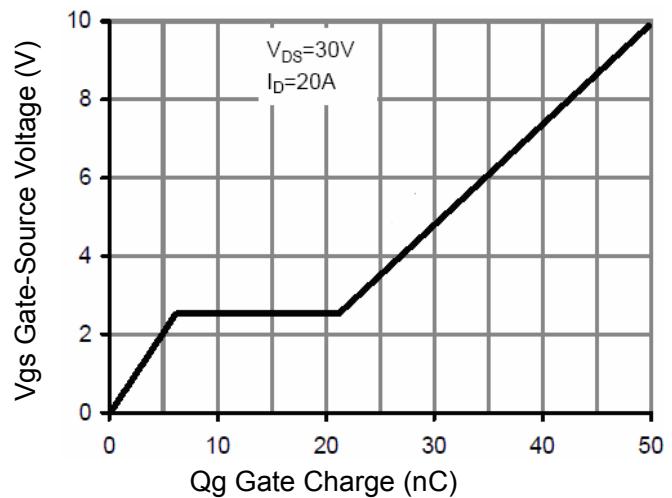
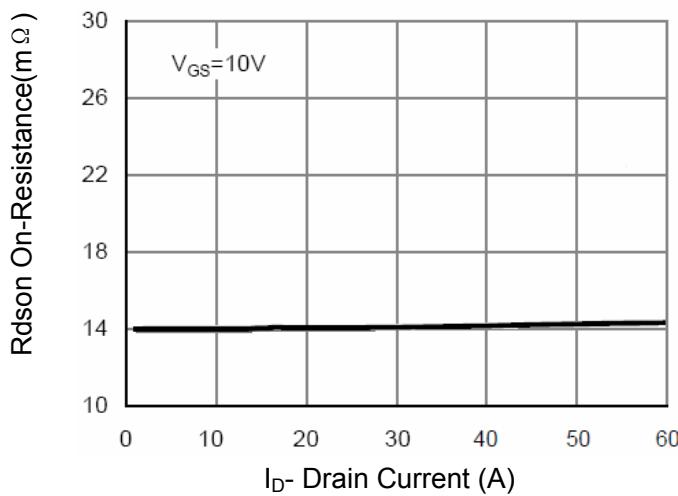
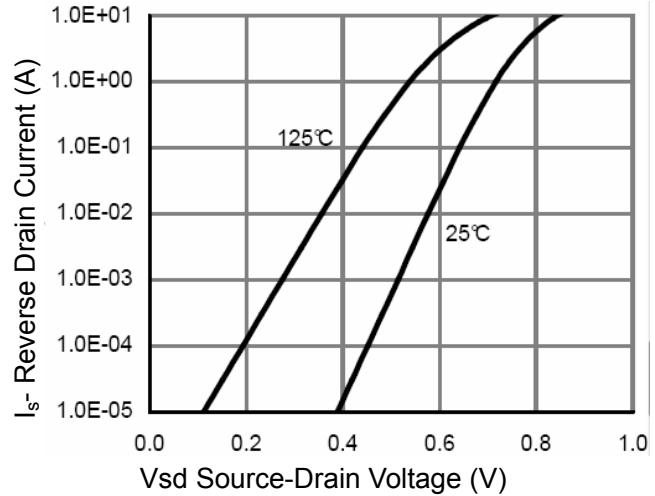


2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

Figure 1 Output Characteristics

Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward

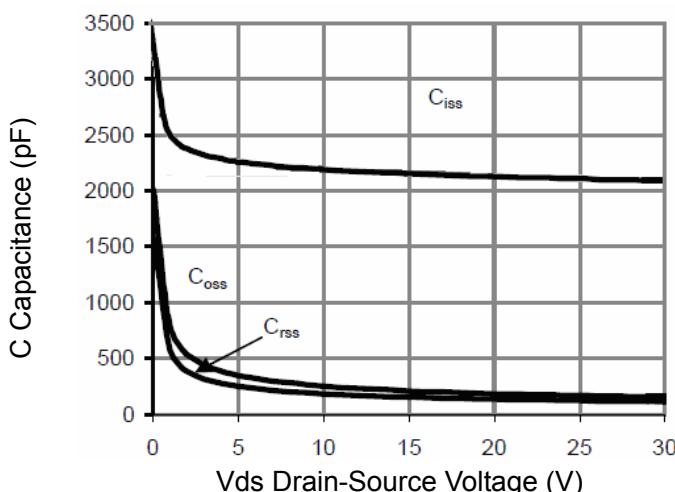


Figure 7 Capacitance vs Vds

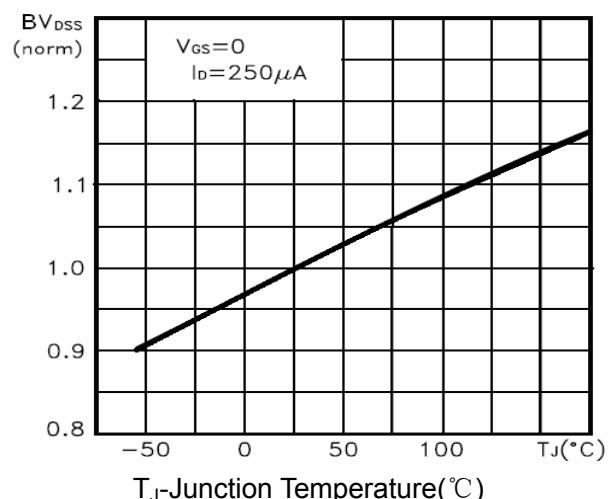


Figure 9 BV_{DSS} vs Junction Temperature

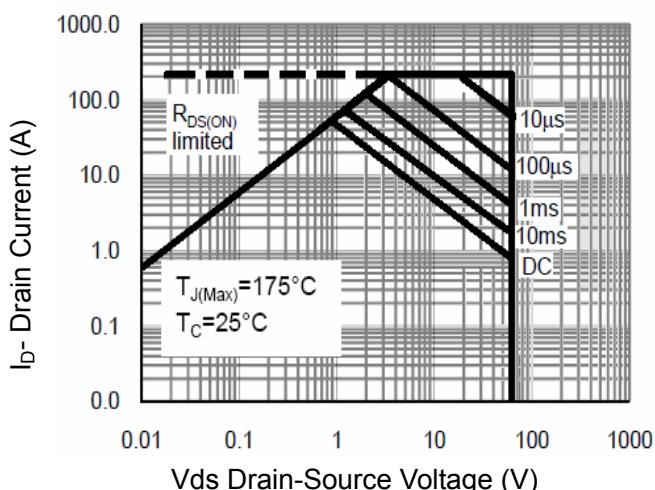


Figure 8 Safe Operation Area

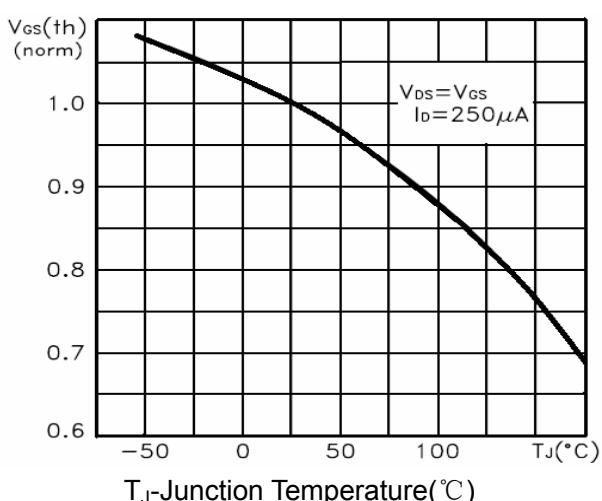


Figure 10 $V_{GS(th)}$ vs Junction Temperature

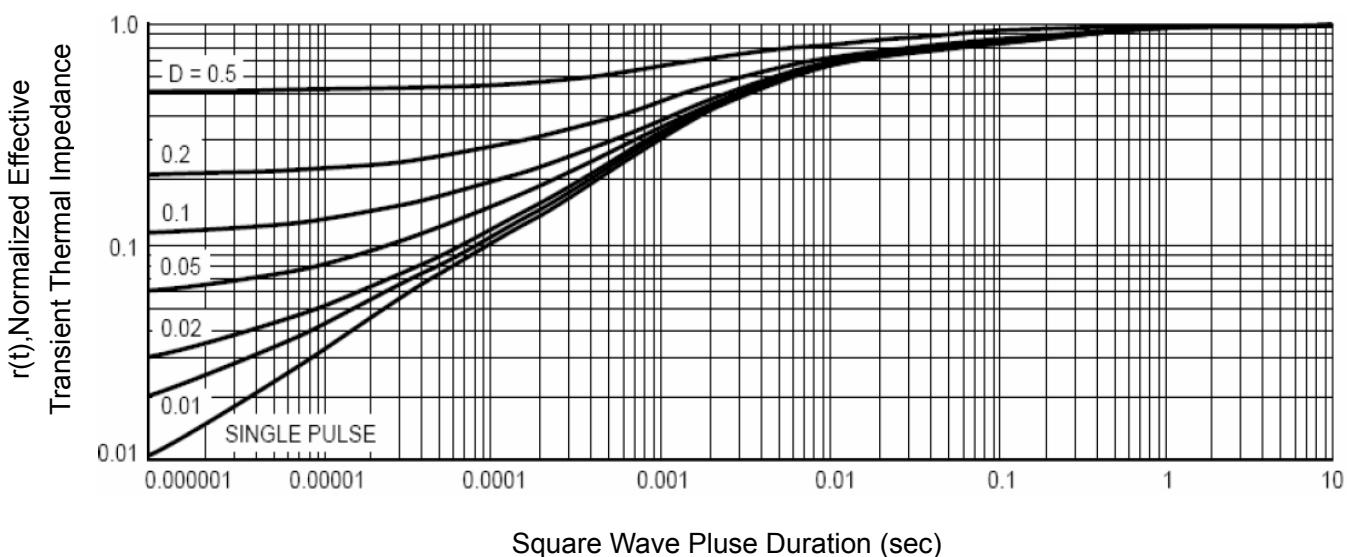


Figure 11 Normalized Maximum Transient Thermal Impedance